REMARKS

Reconsideration of this application, as amended, is respectfully requested. Claims 1-9, 11-33, and 35-50 remain pending. Claims 1-9, 11-33, and 35-50 have been rejected.

Claims 1, 4, 5, 11, 25, 28, 29, and 35 have been amended. Claims 14 and 38 have been cancelled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

REJECTIONS UNDER 35 U.S.C. § 102

Claims 11-24 and 35-48 have been rejected under 35 U.S.C. § 102(e) as being taught by U.S. Patent No. 6,446,198, to Sazegari ("Sazegari").

Applicants have amended claim 11 to include partitioning a look-up memory into a plurality of look-up tables, wherein the look-up memory comprises a plurality of look-up units, and wherein the partitioning of the look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables according a configuration indicator specified by the single instruction.

Sazegari discloses a lookup operation that is carried out by dividing the data table into a number of smaller sets of data that are indexed with a permute instruction (col. 2, lines 17-19). More specifically, Sazegari discloses

> This [permute] instruction operates to fill a register with data values from two other registers. The data values can be specified in any order. Referring to FIG. 3, a permute mask is stored in a register 26, and values that are to be used to form the final result are stored in two data registers 28 and 30. The permute instruction uses the mask values in the register 26 to assign corresponding values of the operands in the registers 28 and 30 to a result register 32...

..For table lookup operations, the permute instruction can be used to perform 16 simultaneous lookup operations on a 32-byte entry table. FIG. 4 illustrates such a table 34, which consists of two 16-byte vectors, data1 and data2. Each vector can be stored in one register of the CPU. The permute instruction can be used to simultaneously read 16 values from these two vectors, in accordance with index values in a register 36, and store the 16 output results in sequential order in another register 38.

(Sazegari, col. 4, lines 7-32(emphasis added)

Further, Sazegari discloses

Since the permute instruction selects bytes from two registers which each have a maximum length of 128 bits, or 16 bytes, it is capable of selecting from among 32 different bytes, or entries in the table. Each of these 32 different entries can be uniquely identified with five bits of each byte in the index register 36. Consequently, the three most significant bits of each byte in this register are unused when the permute instruction is employed for table lookups, as described above. In accordance with the present invention, these three unused bits are employed to expand the size of a table which can be indexed by means of the permute instruction. This result is accomplished through the use of a "select" instruction in combination with multiple permute operations.

(Sazegari, col. 4, lines 33-46)(emphasis added)

Thus, Sazegari merely discloses a data table, which consists of vectors, data 1 and data 2. The permute instruction is used to read values from these vectors. In contrast, amended claim 11 refers to partitioning a look-up memory into a plurality of look-up tables, wherein the look-up memory comprises a plurality of look-up units, and wherein the partitioning of the look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables according a configuration indicator specified by the single instruction.

Therefore, applicants respectfully submit that claim 11 is not anticipated by Sazegari under 35 U.S.C. §102(e).

Given that claims 12-24, 50, 35-48 contain related limitations, applicants respectfully submit that claims 12-24, 50, 35-48 are not anticipated by Sazegari under 35 U.S.C. §102(e).

REJECTIONS UNDER 35 U.S.C. § 103

Claims 1-9, 25-33, and 49 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,446,198 to Sazegari ("Sazegari") in view of U.S. Patent No.

6,397,324 to Barry, et al. ("Barry") and in further view of U.S. Patent No. 5,768,628 to Priem ("Priem").

Applicants respectfully submit that claim 1 is not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Barry, and further in view of Priem.

Amended claim 1 includes the following limitations: receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables; and replacing simultaneously the plurality of entries in the plurality of look-up tables that are indicated by the first plurality of numbers with the second plurality of numbers.

In contrast, none of the references cited by the Examiner discloses such limitations of amended claim 1.

The Examiner acknowledged that "Sazegari has not taught the operation being replacing"(Office Action, page 8, 2/26/07).

In fact, Sazegari discloses a looking up operation using a permute instruction (Sazegari, col. 2, lines 17-43, col. 4, lines 5-67).

Barry, in contrast, discloses splitting a general purpose register files into separate address and computer register files to reduce the number of compute register ports. The portion of Barry, cited by the Examiner (col. 9, line 41-col. 12, line 27) merely discloses storing from the source registers into the tables of elements.

Priem, in contrast, discloses the system memory to store the wave tables (Abstract).

It is respectfully submitted that none of the references cited by the Examiner teaches or suggests a combination with each other. It would be impermissible hindsight based on

applicants' own disclosure, to incorporate the method for storing wave tables of Priem and load and store operations of Barry into the vectorized table lookup of Sazegari. Moreover, such a combination would still lack the following limitations of amended claim 1: receiving a first vector having a first plurality of numbers and a second vector having a second plurality of numbers, each of the first plurality of numbers pointing to one of a plurality of entries, each of the plurality of entries being in one of a plurality of look-up tables; and replacing simultaneously the plurality of entries in the plurality of look-up tables that are indicated by the first plurality of numbers, with the second plurality of numbers.

Given that claims 2-3, and 25-27 contain related limitations, applicants respectfully submit that claims 2-3, and 25-27 are not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Barry, and further in view of Priem.

Applicants respectfully submit that claim 4 is not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Barry, and further in view of Priem.

Amended claim 4 includes the following limitations: receiving the single instruction having an identity number code that specifies a DMA controller and an index of a first entry in a register file that contains control parameters, wherein the control parameters include a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units; receiving the control parameters from the register file; and replacing at least one entry in at least one of the plurality of look-up units in a microprocessor unit according to the control parameters with at least one number using the Direct Memory Access (DMA) controller; wherein the replacing is performed in response to the microprocessor receiving the single instruction.

In contrast, neither of the references cited by the Examiner discloses such limitations of amended claim 4.

The Examiner acknowledged that "Sazegari has not taught the operation being replacing" (Office Action, page 10, 2/26/07).

In fact, Sazegari discloses a looking up operation using a permute instruction (Sazegari, col. 2, lines 17-43, col. 4, lines 5-67).

Barry, in contrast, discloses splitting a general purpose register files into separate address and computer register files to reduce the number of compute register ports. The portion of Barry, cited by the Examiner (col. 9, line 41-col. 12, line 27) merely discloses storing from the source registers into the tables of elements.

Priem, in contrast, discloses the system memory to store the wave tables (Abstract).

It is respectfully submitted that none of the references cited by the Examiner teaches or suggests a combination with each other. It would be impermissible hindsight based on applicants' own disclosure, to incorporate the method for storing wave tables of Priem and load and store operations of Barry into the vectorized table lookup of Sazegari. Moreover, such a combination would still lack the following limitations of amended claim 4: receiving the single instruction having an identity number code that specifies a DMA controller and an index of a first entry in a register file that contains control parameters, wherein the control parameters include a bit segment which specifies a count indicating a number of entries to be loaded in each of a plurality of look-up units; receiving the control parameters from the register file; and replacing at least one entry in at least one of the plurality of look-up units in a microprocessor unit according to the control parameters with at least one number using the Direct Memory Access (DMA) controller; wherein the replacing is performed in response to the microprocessor receiving the single instruction.

Given that claims 5-9, 49, and 28-33 contain related limitations, applicants respectfully submit that claims 5-9, 49, and 28-33 are not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Barry, and further in view of Priem.

The Examiner has rejected claim 50 under 35 U.S.C. § 103(a) as being unpatentable over Sazegari, and in view of Priem.

Applicants respectfully submit that claim 50 is not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Priem.

Amended claim 11 includes the following limitations: partitioning a look-up memory into a plurality of look-up tables, wherein the look-up memory comprises a plurality of look-up units, and wherein the partitioning of the look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables according a configuration indicator specified by the single instruction.

In contrast, none of the references cited by the Examiner discloses such limitations of amended claim 11.

In fact, Sazegari discloses a looking up operation using a permute instruction (Sazegari, col. 2, lines 17-43, col. 4, lines 5-67).

Priem, in contrast, discloses the system memory to store the wave tables (Abstract).

It is respectfully submitted that none of the references cited by the Examiner teaches or suggests a combination with each other. It would be impermissible hindsight based on applicants' own disclosure, to incorporate the method for storing wave tables of Priem into the vectorized table lookup of Sazegari. Moreover, such a combination would still lack the following limitations of amended claim 11: partitioning a look-up memory into a plurality of

look-up tables, wherein the look-up memory comprises a plurality of look-up units, and wherein the partitioning of the look-up memory comprises configuring the plurality of look-up units into the plurality of look-up tables according a configuration indicator specified by the single instruction.

Given that claim 50 depends from amended claim 11, and add additional limitations, applicants respectfully submit that claim 50 is not obvious under 35 U.S.C. § 103(a) over Sazegari, in view of Priem.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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